REMARKS

Claims 42 to 63 remain active in this application of which claims 52 to 63 have been withdrawn from consideration. Claim 42 has been amended to more clearly define the invention.

Claims 42 to 51 were rejected under 35 U.S.C. 102(b) and (e) as being anticipated by Zhang (U.S. 4,750,081), Schroen et al. (U.S. 6,303,977) or Ahn. (U.S. 6,373,109). The rejections ares respectfully traversed.

The invention relates to a structure for minimizing the chip area occupied by the I/O circuitry and an associated ESD device. The I/O structure is disposed at the chip periphery with the ESP device and the core circuitry to which the I/O structure is attached being in the center portion of core of the chip. In accordance with the present invention, this problem is minimized by placing the ESP device or structure at least partially beneath the bond pad on the chip surface at the chip periphery which is part of the I/O structure. No such structure is taught or even remotely suggested by any of the newly cited references. These features are more fully brought out in claim 42 as now amended.

Claim 42 requires, among other features, an electrostatic discharge device disposed in the substrate, the electrostatic discharge device being at least partially disposed beneath the bond pad wherein the bond pad is part of the I/O buffer disposed in the substrate in the peripheral region of the substrate and connected to the bond pad for providing communication between the bond pad and the circuitry, the circuitry positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer. No such combination of features is taught or suggested by Andresen et al. in the combination as claimed. In fact, Schroen et al., which is assigned to the assignee of the

subject application and may come under the provisions of 35 U.S.C> 103(c) does not appear to have ESD protection mentioned and Ahn merely has a gate structure with ESD and nothing more.

Claims 43 to 51 depend from claim 42 and therefore define patentably over Andresen et al. for at least the reasons presented above with reference to claim 42.

Claim 46 further limits claim 42 by requiring that the I/O buffer be a complementary output buffer. No such feature is taught or suggested by the applied references either alone or in the combination as claimed.

Claim 50 further limits claim 42 by requiring that the circuitry be a digital signal processor. No such feature is taught or suggested by the applied references either alone or in the combination as claimed.

Claim 51 further limits claim 42 by requiring that the entire surface of the substrate beneath the bond pad be occupied by the electrostatic discharge device. No such feature is taught or suggested by the applied references either alone or in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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